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09/884,644	06/19/2001	Laurent Guiziou	SP00-131	2645

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EXAMINER	
KIM, RICHARD H	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/884,644	GUIZIOU, LAURENT	
	Examiner	Art Unit	
	Richard Kim	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-4, 6, 21-22, 24 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Lagali et al. (US 6,292,597 B1).

Referring to claim 1, Lagali et al. discloses an optical device comprising a first row of M optical circuit stages, each of the M optical circuit stages being connected to an adjacent optical circuit stage by N parallel waveguides having substantially no curvature (see Fig. 3, ref. 1, 2, 2 x 2 MMIs); and a second row of M optical circuit stages, each of the M optical circuit stages being connected to an adjacent optical circuit by N parallel waveguides having substantially no curvature (see Fig. 3, ref. 3, 4, 2 x 2 MMIs), wherein the first row is coupled to the second row to

form a multi-stage planar device (see Fig. 3, ref. 4 X 4 MMI), and N and M are integers and wherein each of the M optical circuit stages is identical (2 x 2 MMIs).

Referring to claim 2, Lagali et al. discloses an optical device wherein each of the M optical circuit stages includes N-optical circuit units to form and N X N multi-stage planar device (see Fig. 3, ref. MMI).

Referring to claim 3, Lagali et al. discloses an optical device wherein the optical circuit includes a switching device (see col. 8, lines 5-26).

Referring to claim 4, Lagali et al. discloses an optical device wherein the optical circuit includes a Mach-Zehnder switch (see col. 8, lines 5-26).

Referring to claim 6, Lagali et al. discloses an optical device wherein each optical circuit unit includes a directional coupler (see col. 8, lines 15-24).

Referring to claim 21, Lagali et al. discloses a method comprising providing a planar device having a plurality of rows (see Fig. 3, ref. 1-4), each of the plurality of rows having M optical circuit stages (see Fig. 3, 2 x 2 MMIs), each of the M optical circuit stages being connected to an adjacent optical circuit stage by N parallel waveguides having substantially no curvature (see Fig. 3, ref. 1-4), wherein N and M are integers; separating the planar device including a plurality of discrete components, wherein each discrete component includes a row or plurality of rows (see Fig. 3, ref. 1, 2 and 3, 4); and coupling the plurality of discrete components to form a multi-stage planar device (see Fig. 3; ref. 2 x 2 MMIs) and wherein each of the M optical circuit stages is identical (2 x 2 MMIs).

Referring to claim 22, Lagali et al. discloses a method wherein the step of providing includes providing each component with N input waveguides and N output waveguides (see Fig. 3, ref. 1-4).

Referring to claim 24, Lagali et al. a method wherein the step of coupling includes connecting the N output waveguides of a discrete component to the N input waveguides of an adjacent discrete component using a chip-to-chip connection (see Fig. 3, ref. 4, 6).

Referring to claim 28, Lagali et al. discloses a method wherein the planar device is an N x N switch fabric (see Fig. 3).

3. Claims 5, 14 and 29-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lagali et al.

Referring to claim 5, Lagali discloses the device previously recited. However, the reference does not disclose that the switching device includes a Y-digital optical switch.

However, since applicant claims numerous suitable optical circuits, it is a non-critical feature of the invention. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have used any suitable optical circuit stage for the device. Moreover, Applicant has not disclosed that utilizing a Y-switch provides an added advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the Y-switch or the Mach-Zehnder switch disclosed in Lagali. Therefore it would have

been obvious to one having ordinary skill in the art to modify Lagali to obtain the invention as specified in claim 5.

Referring to claim 14, Lagali reference does not disclose that the first row and the second row are connected by optical fibers (see Fig. 3, ref. 26).

Referring to claim 29, Lagali et al. discloses a method comprising the steps of disposing a matrix of optical circuit stages being connected to an adjacent optical circuit stage by N parallel waveguides extending in a first direction to form at least one row of M optical circuit stages, wherein the parallel waveguides have substantially no curvature, and N and M are integers (see Fig. 3) and wherein each of the M optical circuit stages is identical (2 x 2 MMIs). However, the reference does not disclose that the method comprises the step of providing a substrate.

It would have been obvious to one having ordinary skill in the art to provide a substrate in order to provide a base layer for which the circuit is laid out, thereby improving the stability of the device by incorporating all the optical components on one single base layer. Moreover, substrates are well known in the art as a base layer for optical circuits.

Referring to claim 30, Lagali et al. discloses a method comprising the steps of separating the at least one row of M optical circuit stages into a plurality of optical circuit components; and coupling the plurality of optical circuit components to form a multistage planar device (see Fig. 3).

Referring to claim 31-35, Lagali et al. discloses the method previously recited. However, the references do not disclose the method wherein the substrate comprises of silicon, silica, silica material, polymer material or semiconductor material.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the substrate made of silicon, silica, polymer material or semiconductor material since it has been held to be within the general skill of a worker in the art to select a known material on the basis of suitability for the intended use as a matter of obvious design choice. *In re Leshin,* 125 USPQ 416.

Referring to claim 36, Lagali et al. discloses the device previously recited. However, the references do not disclose that the approximate surface area of the substrate is 100mm X 100mm.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the surface area of the substrate to be approximately 100mm X 100mm since one would be motivated to provide a sufficient amount of surface area to accommodate the optical components without significantly decreasing the speed of the device. Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233*

4. Claims 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lagali et al. in view of Edwards et al. (US 6,404,942 B1).

Referring to claim 7, Lagali et al. disclose the device previously recited. However, the references do not disclose the device wherein the optical circuit unit includes a MEMS device.

Edwards et al. discloses a device wherein an optical circuit unit includes a MEMS device (see abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was made for the optical circuit unit to include a MEMS device since one would be motivated to increase the optical switching times (see abstract).

Referring to claims 8-12, Lagali et al. discloses the device previously recited. However, the reference does not disclose the device wherein the optical circuit unit includes a thermo-optical actuator, a mechanical actuator, an electro-optical actuator, an electrostatic actuator or a magnetic actuator.

Edwards et al. discloses a device wherein an optical circuit unit includes an electro-optic actuator, thermo-optic actuator (see col. 1, lines 33-34), magnetic actuator, and an electrostatic actuator (see col. 5, lines 5-10) and a mechanical actuator (see col. 5, lines 52-53).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a thermo-optical actuator, a mechanical actuator, an electro-optical actuator, an electrostatic actuator or a magnetic actuator since one would be motivated to improve the optical switching speed (see abstract).

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lagali et al. in view of Kuroyanagi et al. (US 6,154,583).

Lagali et al. discloses the device previously recited. However, the reference does not disclose that the first row is connected to the second row by a chip-to-chip connection.

Kuroyanagi et al. discloses a device wherein a first row is connected to a second row by a chip-to-chip connection (see Fig. 5, 2nd stage).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the first row connected to the second row by a chip-to-chip connection in order to provide efficient coupling between the optical fibers (see col. 9, lines 17-34).

6. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lagali and Kuroyanagi et al., in view of Douglass (US 5,786,979).

Lagali et al. disclose the device previously recited. However, the references do not disclose the chip-to-chip connection includes a laser weld or an adhesive; and the steps of coupling includes connecting the N output waveguides of a discrete components to the N input waveguides of an adjacent discrete components by laser welding or using an adhesive.

Douglass discloses a chip-to-chip including an adhesive (see col. 5, lines 26-40).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the chip-to-chip connection including an adhesive or laser welding; or the steps of coupling includes connecting the N output waveguides of a discrete components to the N input waveguides of an adjacent discrete components by laser welding or using an adhesive since one would be motivated to improve the durability of the device by retaining the chips in proximate opposition (see col. 5, lines 35-40). Further, since applicant has claimed numerous adhesion techniques, utilizing a laser weld is not a critical limitation, and any suitable adhesion technique can be used to secure the chip-to-chip connection.

7. Claims 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lagali et al. in view of Douglass.

Lagali et al. disclose the device previously recited. However, the references do not disclose the chip-to-chip connection includes a laser weld or an adhesive; and the steps of coupling includes connecting the N output waveguides of a discrete components to the N input waveguides of an adjacent discrete components by laser welding or using an adhesive.

Douglass discloses a device wherein a chip-to-chip connection includes an adhesive (see col. 5, lines 39-40).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the chip-to-chip connection include an adhesive or laser welding; or the steps of coupling includes connecting the N output waveguides of a discrete components to the N input waveguides of an adjacent discrete components by laser welding or using an adhesive since one would be motivated to improve the durability of the device by retaining the chips in proximate opposition (see col. 5, lines 35-40). Further, using either a laser weld or adhesive would be obvious since neither one of the actuating mechanisms provides a significant advantage over the other, and using either one maintains the primary purpose of the device.

7. Claim 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Lagali et al. and Kuroyanagi et al., in view of Dannoux et al. (US 5,447,585).

Lagali et al. discloses the device previously recited. However, the references do not disclose that the chip-to-chip connection is implemented using a mass pigtailing technique.

Dannoux et al. discloses a mass pigtailing technique (see abstract).

It would have been obvious to one having ordinary skill in the art to implement a mass pigtailing technique in the chip-to-chip connection since one would be motivated to facilitate to facilitate optical connections during active alignment and measurement testing (see abstract).

8. Claim 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lagali et al. and Kuroyanagi et al., in view of Graves (US 6,366,716 B1).

Referring to claim 19, Lagali et al. and Kuroyanagi et al. disclose the device previously recited. However, the references do not disclose the chip-to-chip connection includes aligning and mounting the first row and second row on an alignment substrate.

Graves et al. discloses a device wherein the optical components are disposed on an alignment substrate (see col. 3, lines 44-49).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the chip-to-chip connection include aligning and mounting the first row and second row on an alignment substrate since one would be motivated to increase the ease of aligning the optical components with one another, thereby adding precision to the device. According to Graves et al. "Implementing the optical switching devices as monolithic structures on silicon wafers allows alignment features to be provided such that components of the device can be positioned and interconnected within required tolerances" (see col. 3, lines 44-49).

Referring to claims 20, Lagali et al. and Kuroyanagi et al. disclose the device and method previously recited. However, the references do not disclose the device wherein an index-matching material is disposed between the first and second rows.

Graves et al. discloses a device and method wherein an index-matching material is disposed between optical components (see col. 14, line 20).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have an index-matching material disposed between the first and second rows in order to reduce coupling loss between the first and second row. According to Graves et al., such a modification would provide a continuous optical path therethrough (see col. 14, lines 20-23), thereby preventing coupling loss due to discontinuity within the path that could arise due to variations of the refractive index.

8. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lagali et al. in view of Graves et al.

Lagali et al. discloses the method previously recited. However, the references do not disclose the method wherein an index-matching material is disposed adjacent discrete components.

Graves et al. discloses a device and method wherein an index-matching material is disposed between optical components (see col. 14, line 20).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have an index-matching material disposed between discrete adjacent components in order to reduce coupling loss between the first and second row. According to Graves et al., such a modification would provide a continuous optical path therethrough (see col. 14, lines 20-23), thereby preventing coupling loss due to discontinuity within the path that could arise due to variations of the refractive index.

Response to Arguments

9. Applicant's arguments filed 3 September 2003 have been fully considered but they are not persuasive.

10. In response to Applicant's argument that Lagali does not describe or suggest the device *wherein each of the M optical circuit stages are identical...*, Examiner asserts that the optical stages shown in Figure 3 of Lagali are indicated as identical since both are 2 x 2 MMI optical circuits.

11. In response to Applicant's argument that Lagali fails to include a switching device including a Y-digital optical switch, Examiner asserts that such a limitation is obvious according to the rejection above. Moreover, Lagali clearly discloses the first row connected to the second row by optical fibers in Fig. 3, ref. 26.

12. In response to Applicant's argument that Lagali does not disclose that the method comprises the step of providing a substrate, Examiner asserts that providing a substrate is well known in the art, as further indicated by the Edwards reference.

13. In response to Applicant's argument that Lagali or Edwards, do not describe or suggest a thermo-optical actuator, a mechanical actuator, an electro-optical actuator, an electrostatic actuator or a magnetic actuator, Examiner asserts that those limitations are clearly disclosed in the Edwards reference as described in the rejection above. Moreover, even if the Edwards reference does not disclose one or more of the above actuators, since applicant has disclosed numerous different types of actuator that can be used, without stating a clear advantage of using

one over other, the type of actuator used is not a critical limitation, and any suitable actuator can be used to actuate the optical switch.

14. In response to Applicant's argument that the Lagali or Kuroyanagi references do not disclose a first row connected to a second row by a chip-to-chip connection, such a limitation is indicated in Figure 5 of the Kuroyanagi reference with motivation to combine the Lagali reference and Kuroyanagi reference indicated in the above rejection.

15. In response to Applicant's argument that the references do not provide motivation to add a Douglass type adhesive, Examiner asserts that such a motivation is suggested in col. 5, lines 35-40 of Douglass. Moreover, utilizing a laser weld would be obvious according the above rejection.

16. In response to Applicant's argument that the references do not disclose a chip-to-chip connection implementing a mass pigtailing technique, Applicant asserts that such a limitation is disclosed in Dannoux, with the motivation to combine described in the abstract.

17. In response to Applicant's argument that the references do not disclose an index-matching material, Examiner asserts that such a limitation is disclosed in the Graves reference. Motivation to combine is describe in the above rejection.

18. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

19. Applicant's arguments with respect to claims 1-12 and 14-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Kim whose telephone number is (703)305-4791. The examiner can normally be reached on 9:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H Kim can be reached on (703)305-3492. The fax phone number for the organization where this application or proceeding is assigned is (703)308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Richard Kim
Examiner
Art Unit 2871

RHK

T. Chowdhury
Primary Examiner